



**PICMG® COM.0  
COM Express™ Module Base Specification  
Errata Notification COM.0-R1.0-ERRATA002**

**December 20, 2006**

**Affected Specification:**

PICMG® COM.0 COM Express™ Module Base Specification Revision 1.0, July 10, 2005

**Errata Description:**

**E01)** From Errata Notification COM.0-R1.0-ERRATA001, December 6, 2005.

On Table 4-1 on page 27 of the subject specification, the description of the **KBD\_A20GATE** signal incorrectly states the direction of the pull down resistor on the module.

**Change from:**

Miscellaneous	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
KBD_A20GATE	I CMOS	3.3V / 3.3V	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC-AT. Pulled <b>low</b> on the module.	All

**Change to:**

Miscellaneous	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
KBD_A20GATE	I CMOS	3.3V / 3.3V	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC-AT. Pulled <b>high</b> on the module.	All

**E02)** New in Errata Notification COM.0-R1.0-ERRATA002, December xx, 2006.

In Table 4-1 on page 28 of the subject specification, the description of the **PWRBTN#** signal incorrectly states the active edge of the signal.

**Change from:**

Miscellaneous	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
PWRBTN#	I CMOS	3.3V / 3.3V Suspend	Power button to bring system out of S5 (soft off), active on <b>rising</b> edge.	All

**Change to:**

Miscellaneous	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
PWRBTN#	I CMOS	3.3V / 3.3V Suspend	Power button to bring system out of S5 (soft off), active on <b>falling</b> edge.	All

**E03)** New in Errata Notification COM.0-R1.0-ERRATA002, December xx, 2006.

In Table 4-1 on page 28 of the subject specification, the description of the **SUS\_S5#** signal erroneously implies SUS\_S5# and the ATX PS\_ON signal are synonymous.

**Change from:**

Miscellaneous	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SUS_S3#	O CMOS	3.3V / 3.3V Suspend	Indicates system is in Suspend to RAM state. Active low output.	All
SUS_S4#	O CMOS	3.3V / 3.3V Suspend	Indicates system is in Suspend to Disk state. Active low output.	All
SUS_S5#	O CMOS	3.3V / 3.3V Suspend	Indicates system is in Soft Off state. <b>Also known as "PS_ON" and can be used to control an ATX power supply.</b>	All

**Change to:**

Miscellaneous	Pin Type	Pwr Rail / Tolerance	Description	Pin Availability
SUS_S3#	O CMOS	3.3V / 3.3V Suspend	Indicates system is in Suspend to RAM state. Active low output. <b>An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.</b>	All
SUS_S4#	O CMOS	3.3V / 3.3V Suspend	Indicates system is in Suspend to Disk state. Active low output.	All
SUS_S5#	O CMOS	3.3V / 3.3V Suspend	Indicates system is in Soft Off state. <del>Also known as "PS_ON" and can be used to control an ATX power supply.</del>	All